

REMARKS

Claims 1-30 have been examined and are now pending in the application. Claims 1, 3-4, 7-7 and 9-13 are amended. Reexamination and reconsideration of all outstanding rejections and objections are requested.

Claims 1-13 and 17-30 are rejected under 35 U.S.C. §103(a) as being unpatentable by Hayter et al. in view of Mann

Claim 1 recites an interface for a network device and a CPU, with the interface including a shared memory including a Rx buffer pool, maintained in the shared memory and which is write-only by the CPU and read-only by the device, comprising a plurality of buffer pool entries, each entry holding an address and length value of a scatter-gather buffer; a transmit FIFO pool which is write-only by the CPU and read-only by the device, with each FIFO pool entry holding a buffer length, start field, end field, and buffer address field; a status ring, maintained in shared memory and which is read-only by the CPU and write-only by the device, with each status ring entry holding status information written by the device and a toggle bit which holds a value which is changed by the device each time the device accesses the status ring; and a private memory, accessible only by the CPU, with the private memory holding a shadow copy of the scatter/gather buffers, in software-friendly form, included in the received buffer pool and a shadow count of the number of available of Tx FIFO entries.

The reference Hayter discloses a system for packet processing. In Hayter when a packet is received the packet interface circuit selects a descriptor for the packet and may update a descriptor when a packet is complete. [0027]

Mann discloses a debug trace controller. An instruction trace configuration register (ITCR) is described which includes a TX bit (27) which indicates that the target system 111 is ready to transmit data to the host system and the data is available in the TX_DATA register and also includes an RX bit (26) which indicates that data has been received from the host and placed in the RX_DATA register. (9:56 to 10:35). A debug control/status register (DCSR) includes an RX bit that indicates that data has been received from the host and placed in the RX_DATA register. (10:38 to 10:65).

The processor core initiates a data transmission by first testing the read-only TX bit in the IRCR register. (33:24). The host systems data to the processor core by first testing the read-only RX bit in the DCSR register. (33:39).

The examiner states that, as per claim 1, Hayter discloses the invention substantially as claimed except that Hayter does not disclose an RX buffer pool which write-only by the CPU and read-only by the device and a transmit buffer pool that read-only by the device. It is further stated that Mann teaches these missing elements citing col. 33, lines 38-40 and col. 33 lines 23-35)

This rejection is respectfully traversed for the following reasons.

The establishment of a *prima facie* case of obviousness requires that all the claim limitations must be taught or suggested by the prior art. MPEP §2143.03

The claimed element of a status ring, independent of the Rx buffer pool and Tx FIFO pool is not disclosed in Hayter or Mann. As described above, in Hayter the packet interface unit updates the descriptor. This is the same descriptor that is used for transmit and receive. There is not separate status ring.

The Rx buffer pool which is write-only by the CPU and read-only by the device and comprises a plurality of buffer pool entries each entry holding an address and length value is not disclosed by Mann.

The part of Mann cited by the examiner as being the read-only by the device refers to a status bit in the DCSR register. This status bit does not hold an address and length value as recited in claim 1. Accordingly, the Rx buffer pool is not fairly taught or suggested by Mann.

The part of Mann cited by the examiner as being the transmit buffer pool which is write-only by the CPU and read-only by the device is a status bit in the ITCR register. This status bit does not hold an address and length value as recited in claim 1. Accordingly, the Rx buffer pool is not fairly taught or suggested by Mann.

The registers of Mann pointed to in the office action can not be substituted into Hayter to achieve the functionality of pointing to scatter/gather buffers used to hold transmit and receive packets.

The recited private memory, accessible only by the CPU, with the private memory holding a shadow copy of the scatter/gather buffers, in software-friendly form, included in the received buffer pool and a shadow count of the number of available of Tx FIFO entries is not found in Hayter or Mann. All the citations in the office action refer to either the L2 cache 14 or Memory 28. Neither of these structures include the private memory recited in claim 1.

The interface described in Hayter is the same as the conventional interface depicted in Fig. 1 of the present application and described at paragraphs [42]-[43].

Accordingly, Hayter and Mann, singly or in combination, do not fairly teach or suggest the limitations recited in claims 1

Independent claims 3, 4, 6, 7, 9, 10, 11, 12, and 13 recite similar limitations as claim 1 and are allowable for the same reasons. Claims 2, 5, 8 are dependent claims which are allowable for the same reasons as the independent claims from which they depend.

Claim 17 recites a system for transferring transmit packet data to a transmit interface, that comprises a processor module including a processor and a data mover, with the data mover having access to the module internal resources; a memory holding a transmit ring and buffers, with each transmit ring entry for holding an address of a transmit buffer, and with the memory holding a data mover descriptor ring which is initialized by the processor; a high-speed bus coupled to the memory and the processor module; an interface module coupling the high-speed bus to the transmit interface, with the interface module responding to a transmit indication to read a transmit ring entry from the memory, to translate a transmit ring entry into a data mover descriptor, to write a translated data mover descriptor to the data mover descriptor ring for each transmit ring entry of a packet to be transmitted, to write a terminator descriptor to the data mover descriptor ring when the end of the packet is detected, and then to signal the data mover to read the data mover descriptors from the data mover descriptor ring; and with the data mover initiating packet data transfer to the interface module when signaled by the interface module.

The examiner states that the subject matter recited in claim 14 is disclosed in Mann: col. 21, lines 19-30.

Referring to the citations in the office action, a useful debug function to account for segment changes that occur while tracing is stopped is described. As is known in the art, Intel processors use a segmented memory management technique with segment addresses held in the processor.

The function is performed by selecting an option to report the segment base address and segment attributes of the current code segment. The segment attributes report status for paging (PG), operand sizes (SZ), and addressing modes (R/P).

The claimed interface module the with the interface module responding to a transmit indication to read a transmit ring entry from the memory, to translate a transmit ring entry into a data mover descriptor, to write a translated data mover descriptor to the data mover descriptor ring for

each transmit ring entry of a packet to be transmitted, to write a terminator descriptor to the data mover descriptor ring when the end of the packet is detected is not found in Mann.

Accordingly, the limitations recited in claim 17 are not fairly taught or suggested by the cited references.

Claims 18, 20, 22 are independent claims that recite limitations similar to those described above in claim 17. Accordingly, those claims are allowable for the same reasons as claim 17. Claims 19, 21, and 23 are dependent claims allowable for the same reasons as the claims from which they depend.

Claim 25 recites a method for implementing packet transmit flow control in a system including a processor, memory, and interface module, coupled by a high-speed bus, with the interface module able to directly access processor memory and interfacing the high-speed bus with transmit interfaces, and with memory holding an xon/xoff table and an xon status ring initialized by the processor, said method comprising the steps of: at the interface module, maintaining the xon/xoff table to indicate the current xon/xoff transmit status of the transmit interfaces, writing an entry to the xon status ring indicating an interface that transitions from xoff to xon, and interrupting the processor subsequent to writing to the xon status ring; and at the processor, responding to the interrupt to read the xon entry, checking whether packets are holding to transmit over the identified interface, and indicating to the interface module when the xon status ring entry has been processed.

The office action cites Mann: col. 25, Table 2 as having a status capture for the user, col. 25, lines 45-62.

Table 25 of Mann describes bond-out signals only available on special parts. Col 25, lines 45-62 a flow chart of the host/serial port interface of the JTAG TAP controller 204. A instruction is written using a shift instruction and the Pending flag is cleared and Finish flag is asserted.

A slave copy is maintained due to the possibility of the status changing between the Capture-DR and Update-DR TAP controller states. The processor saves the slave copy to determine the status the user will detect at the time the status capture is performed to prevent the loading of the next instruction if the user sees that the previous instruction has not finished.

The claimed maintaining an xon/xoff table at an interface module, writing an entry to the xon status ring indicating an interface that transitions from xoff to xon, and interrupting the processor subsequent to writing to the xon status ring; and at the processor, responding to the interrupt to read the xon entry, checking whether packets are holding to transmit over the identified

interface, and indicating to the interface module when the xon status ring entry has been processed are not found in Mann.

There is no disclosure of an xon/xoff table in Hayter or of the claimed steps. Hayter only discloses a Pending flag and a Finish flag set by processor included in an instruction loaded using a shift register.

Independent claims 24, 27 and 29 recite limitations similar to those described above in claim 24 and are allowable for the same reasons. Dependent claims 26, 28, and 30 are allowable for the same reasons as the claims from which they depend.

Claims 14-16 are rejected under 35 U.S.C. §102(e) as being anticipated by Zhao.

Claim 14 recites a method for fairly allocating receive buffers in an interface between a plurality of line cards and a CPU, where interface includes a like plurality of budget counters holding LC budget value, each associated with a particular line card, and a receive buffer counter holding a receive buffer value indicating a number of available receive buffers for holding packets received at the line card. The method comprises the following steps implemented at the CPU. Initializing each LC budget value to a ratio of the bandwidth of the line card associated with the budget counter to the total bandwidth of all line cards coupled to the interface, scaled to a number of receive interface buffer resources available to the interface; incrementing the LC budget value associated with a particular line card when the CPU processes a receive buffer holding packet data stored by the particular line card; incrementing the receive buffer when the CPU processes a receive buffer holding packet data; decrementing the LC budget value associated with a particular line card when the interface receives packet data from the line card and places the packet data in a receive buffer; decrementing the receive buffer when the interface receives packet data from a line card and places the packet data in a receive buffer; and dropping packets from a line card when the associated LC budget value is zero or less.

Zhao teaches a switch queue predictive protocol. In Zhao each line card maintains a table of predicted available queue space for the associated cross-point queue in the switch fabric. The entries to the table are predictive queue spaces (PSQs) and each PSQ value is originally set the size of the buffer. A PSQ is decremented when a linecard sends a packet to a particular queue and can only send a packet when PSQ is not zero. (7:39 to 8:18)

An egress queue management block detects congestion and when congestion is detected sends an egress congestion indication for the transmit queue. If a source linecard attempts to send packets to queue that is congested its PSQ value will go to zero and no more packets are sent

to the queue. If the congestion condition is removed the PSQ value will be updated to a value greater than zero and the source linecard will again transmit packets to the queue.

The basic requirements for anticipation are set forth in MPEP §2131: A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.

There is no description in Zhoa of the claimed step of initializing each LC budget value to a ratio of the bandwidth of the line card associated with the budget counter to the total bandwidth of all line cards coupled to the interface, scaled to a number of receive interface buffer resources available to the interface.

In Zhoa each PSQ value is set to the size of the buffer. Thus, the advantage of the claimed system of preventing starvation of a low bandwidth linecard by a high bandwidth linecard.

Accordingly, every element of claim 14 is not expressly or inherently described by Zhoa.

Claims 15 and 16 recite limitations similar to claim 14 and are allowable for the same reasons.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

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If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (925) 944-3320.

Respectfully submitted,

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